

AG-5
Averaging Frame Grabber
PCI Version

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Communications Regulations

FCC Statement

This equipment has been tested and found to comply with the limits for a Class B digital device in accordance with the specifications in Part 15 of FCC rules. See instructions if interference to radio or television reception is suspected.

Radio and Television Interference

The equipment described in this manual generates, uses, and can radiate radio frequency energy. If it is not installed and used properly, it may cause interference with radio and television reception. This equipment has been tested and found to comply with the limits for a Class B digital device in accordance with the specifications in Part 15 of FCC rules. These specifications are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation.

You can determine whether your computer system is causing interference by turning it off. If the interference stops, it was probably caused by the computer or one of the peripheral devices.

If your computer does cause interference to radio or television reception, try to correct the interference by using one or more of the following measures:

- Turn the television or radio antenna until the interference stops.

- Move the computer to one side or the other of the television or radio.

- Move the computer farther away from the television or radio.

- Plug the computer into an outlet that is on a different circuit from the television or radio.

If necessary, consult Scion or an experienced radio/television technician for additional suggestions. You may find the following booklet helpful: *Interference Handbook* (stock number 004-000-00493-1). This booklet, prepared by the Federal Communications Commission, is available from the U.S. Government Printing Office, Washington, DC 20402.

Changes or modifications to this product not authorized by Scion Corporation could void the FCC Certification and negate your authority to operate the product.

Getting Started

Introduction

The AG-5 frame grabber that you have just received is a high-quality instrument suitable for use in a variety of scientific and industrial imaging applications such as video microscopy, autoradiography, and automatic process inspection. The primary function of the AG-5 is to capture video frames from standard RS-170 (or CCIR) video sources such as CCD cameras. The AG-5 is supplied with Scion Image, a version of the popular image acquisition and analysis software package, NIH Image, developed at the National Institutes of Health. Scion Image is a slightly extended version of NIH Image that supports additional features of the AG-5 as well as other Scion imaging boards. The AG-5 also comes with a PhotoShop module for use with other software packages that support the PhotoShop interface.

The AG-5 has numerous features, besides an exceptionally clear and sharp picture, that are particularly useful for demanding scientific use. The AG-5 is capable of a real-time video display rate of 30 frames per second on the Macintosh monitor. It is also capable of capturing frame sequences to Macintosh system memory at 30 fps. The AG-5 allows real-time frame averaging and frame summation which are particularly useful for noisy or low-light imaging. In addition real-time arithmetic and logical operations such as background subtraction are supported. Frame capture may be controlled by an external trigger signal. The AG-5 allows software control of the range of digitization of the video signal, which provides an analog offset and gain capability. Also, the AG-5 has a dedicated open drain output that may be used with Scion Image to control several on-chip integrating cameras.

Please take a few moments to read through this manual before you begin using your AG-5 as it should answer some of the questions that you may have concerning your new frame grabber. Please contact us at Scion Corporation should you encounter difficulty at any time, or if you have any questions.

Contents

You have received in addition to your AG-5 frame grabber: a CD-ROM, and an installation sheet. You may also have received a cable to connect a video source to the frame grabber board. All cables are optional.

The CD-ROM contains a short Read Me file, this manual, the driver file for the frame grabber, a compressed archive containing the Scion Image application program along with complete documentation. Should any items be missing, please contact Scion Corporation so that we can rush you the missing items.

System Requirements

The AG-5 can be installed in any Macintosh with a full-sized PCI slot. This includes all currently shipping PCI Macintoshes – the Power Macintosh 7200, 7500, 8500, and 9500.

Any standard RS-170 (or CCIR) video source can be used with the AG-5. The RS-170 (CCIR) standard is a specification for monochrome video signals. The AG-5 board does

not come standard with a cable. An optional cable can be purchased from Scion Corporation. The AG-5 cannot be directly connected to a color (NTSC or PAL) video signal. The color information in a color video signal will produce an unacceptable interference pattern in captured frames. The AG-5 can, however, be connected to RGB video sources using the optional RGB cable. When connected to an RGB source, the AG-5 can capture frames from each of the individual color signals and can capture three-pass color images.

The AG-5 is designed for use primarily with RS-170 (or CCIR) CCD cameras and RGB output CCD cameras. The AG-5 does not perform time-base correction on the incoming video signal. This means that the AG-5 may have sync difficulties with some consumer quality VCR's and camcorders that exhibit large time-base errors.

Installation

AG-5 Circuit Board

Installing the AG-5 in your Macintosh is an easy process that should only take a couple of minutes. The first step is to remove the cover from your Macintosh. If a PCI card retainer is present, swing it aside so that the PCI slots are accessible. If you are unsure of the proper method for removing the cover from your particular Macintosh, consult your Macintosh user's manual. Once the PCI slots are exposed, select the PCI slot that you wish to use and, if necessary, remove the cover from the opening in the rear of the Macintosh case that corresponds to the slot.

At this point, make sure that you have discharged all static electricity from your body. A good way to discharge static electricity is to touch the Macintosh power supply. Remove the AG-5 frame grabber from its static shielding bag. Holding the AG-5 by its top edge, align the rear edge of the circuit board with the card guide corresponding to the selected slot. At the same time, align the AG-5's connector bracket with the slot opening. When the circuit board is aligned, carefully lower the AG-5 into the slot until the edge connector on the bottom of the board rests against the Macintosh PCI connector. Check to insure that the board and the connector are appropriately aligned. Then press firmly on the top edge on the circuit board until the board mates with the connector. If excessive force is required to mate the connectors, remove the AG-5 from the Macintosh and try again. Once the AG-5 is inserted in the PCI slot, replace the PCI card retainer, if present, then replace the cover of your Macintosh.

Cables

If you bought the Single Source cable then insert the nine pin connector of the cable into the nine pin connector of the AG-5. When the connectors are mated, tighten the two screws on the single source cable connector. Connect the BNC end of the single source cable to your camera. If you are using the RGB cable, it connects to the AG-5 in the same manner as the single source cable. Connect the nine pin connector to the nine pin connector of the AG-5. The other end (or ends) of the cable connects to your video source. If you have a video source with a non-standard connector, please contact Scion for assistance.

Scion Image Software

To install the Scion Image software package, insert the Scion CD-ROM and double click the Scion Image folder. To decompress the archive, double click on the archive icon and follow the directions. The archive will decompress into a Scion Image folder containing the program as well as documentation, sample macros, and convolution kernels.

There are four Adobe PDF documents describing the Scion Image package. 'NIH Image Manual' is the user's manual for the standard version of NIH Image. 'NIH Image Engineering' is a brief introduction to some of the technical aspects of imaging. 'Inside NIH Image' describes some of the structure of the standard Image program and discusses ways to modify it for custom applications. All of these documents apply to Scion Image as well. The final document, 'Mods to NIH Image' describes the extensions to the standard Image that are available in Scion Image and how to use them.

Using the AG-5

Introduction

Once the AG-5 circuit board has been installed, the supplied single source cable connected to the AG-5 and your camera, and the Scion Image archive copied to your hard disk and decompressed, you are ready to begin using your AG-5. This section will describe some of the capturing capabilities of the AG-5 and Scion Image – such as normal grayscale capturing, frame averaging, arithmetic and logical operations, color capturing, and using the external trigger.

Once the Scion Image software has been started, by double clicking on the program icon, the Scion Image menus and windows will be presented. The commands that deal with the AG-5 and image capturing, such as basic grayscale capturing, frame averaging, arithmetic and logical operations, and color capturing, are contained in the 'Special' menu and the 'Stacks' menu.

Grayscale Capturing

When the 'Start Capturing' command, under the 'Special' menu, is selected, the program will continuously capture and display video frames. The display rate on all current Macintosh models is 30 frames per second. On some Macintoshes, it may be necessary to move the cursor out of the image window to achieve the maximum display rate. You may stop the continuous capture process at any time by either choosing the menu command again (which has changed to 'Stop Capturing') or by clicking in the 'Camera' window with any of the tools except the magnifying glass or the grabber. Once the capturing process has stopped, the captured frame is available for analysis or saving to disk.

The 'Video Control' dialog box, also under the 'Special' menu, allows you to change various parameters of capture. The 'Offset' and 'Gain' fields allow you to adjust the range of digitization of the AG-5's analog to digital converter. 'Use External Trigger' enables the AG-5's external trigger capability. 'Video Rate Math' enables real-time arithmetic and logical operations. 'Video Rate Blank Field' enables real-time blank field shading correction. 'Separate Sync' should be enabled when the AG-5 is connected to an RGB video source using the optional four source cable. It instructs the AG-5 to look for video sync information on the sync channel of the four source cable. The 'Channel' radio buttons select which of the AG-5's four video sources is to be digitized.

Frame Averaging and Summation

The 'Average Frames' command is useful for reducing random video noise or accumulating low-light images. This command is also found under the 'Special' menu. The AG-5 is capable of averaging or summing at 30 frames per second. To enable real-time averaging or summation, check the 'Video Rate' box in the 'Average Frames' dialog box. The number of frames to average or sum can be specified from 2 to 127 frames.

To sum frames, instead of averaging, check the 'Integrate' box in the 'Average Frames' dialog box. The AG-5 will sum the specified number of frames at video rate and then scale the accumulated pixel values to the range 1 to 254. The AG-5 accomplishes the scaling by keeping track of the smallest and largest accumulated pixel values and linearly scaling the range between them. If the 'Fix Scale' box is checked, then the scaling process may be

user controlled. Minimum and maximum accumulated pixel values may be entered in the appropriate boxes and this range will be linearly scaled to the range 1 - 254. The AG-5 will set all accumulated pixels less than the specified minimum to 0 and all pixels greater than the specified maximum to 255.

The 'Integrate on-chip' allows the use of integrating cameras. The specified number of frames will be integrated on the imaging sensor of the camera and the resultant image will then be captured by the AG-5. Currently supported integrating cameras are the Cohu 491X series and the Dage CCD-72. An optional cable, CAB-DAGE-AG5, will be required for connecting the AG-5 to the integration input of the Dage Camera. The Cohu adapter, CAB-COHU-ADP will adapt the Dage cable for the Cohu 491X.

Arithmetic and Logical Operations

The AG-5 is capable of performing arithmetic and logical operations between incoming raw video and a stored reference frame. This feature is enabled by the 'Video Rate Math' box in the 'Video Control' dialog box. Once this box is checked, the operation to perform may be specified by the 'Video Math' menu command under the 'Special' menu. The 'Video Math' command will allow the specification of a window to use as a reference frame, the operation to be performed, and gain and offset factors. If a valid configuration has been specified by the 'Video Math' command, and the 'Video Rate Math' box has been checked, all subsequent captured frames will be processed by the AG-5 according to the specified operation.

To disable video rate arithmetic and logical operations, uncheck the 'Video Rate Math' box. Video rate processing can also be temporarily disabled by holding down the 'Control' key while frames are being captured. Note that the operation being performed can be changed at any time by selecting the 'Video Math' command.

Blank Field Shading Correction

The AG-5 is also capable of real-time correction of images for variations in lighting or camera response. To enable this feature, check the 'Video Rate Blank Field' box in the 'Video Control' dialog box. Then capture a frame of the blank field and load it into the AG-5 using the 'Save Blank Field' menu command under the 'Special' menu. All subsequent captured frames will be corrected for shading variations. For more information on blank field correction, refer to the description of the 'Save Blank Field' command in the Image manual.

To disable real-time blank field correction, either uncheck the 'Video Rate Blank Field' box or close the 'Blank Field' window. Video Rate Blank Field correction may be temporarily disabled by holding down the 'Control' key. Note that video rate blank field correction and video rate arithmetic and logical operations can not both be active at the same time.

Color Capture

The 'Capture Color' command, under the 'Stacks' menu, will capture a three-pass 24 bit color image using the AG-5. To capture color, you must have the optional four source cable connected to an RGB video source and the 'Separate Sync' box checked in the 'Video Control' dialog box. When the command is selected the software will capture three separate frames using the AG-5. The first frame will be captured from the red video signal, the second frame from the green video signal, and the third frame from the blue video signal.

After the 'Capture Color' command has completed, there will be a three slice stack on the screen and an 8 bit indexed color image. This stack will contain the three color slices – red, green, and blue. The 8 bit indexed color image represents the captured 24 bit color image. The 8 bit color look-up table used to display the 8 bit indexed image may be selected using the 'RGB to 8-bit Color' command.

External Triggering

The AG-5 has an external trigger capability that allows the synchronization of frame capture to external events. The external trigger feature is enabled in the 'Video Control' dialog box as discussed above. When this feature is enabled, the AG-5 will wait for a trigger event on its external trigger input before capturing a frame. A trigger event is defined as a falling TTL edge (that is, a transition from 5 volts to 0 volts). The trigger input is pin 9 of the 9 pin video connector. Once the trigger event has occurred, this input must be brought back to 5 volts before another trigger event can be recognized.

Architectural Description

Overview

The hardware architecture of the AG-5 is designed to provide advanced image processing features and maximum flexibility, combined with a simple programming interface. Such features include separate multiplexors for video information and for sync information, 8 bit digital to analog converters for controlling the range of digitization, an input look-up table, an arithmetic/logical operation look-up table, frame accumulation, and quick division and scaling of the accumulation buffer.

The programming interface of the AG-5 consists of six control registers, one status register, an accumulation minimum and an accumulation maximum register, an input look-up table, an arithmetic/logical operation look-up table, four 8 bit frame buffers, and one 15 bit accumulation buffer. The registers, the frame buffers, and the accumulation buffer are available to the programmer at all times, even during digitization. Hence software can be transferring one frame from the AG-5 to system memory at the same time that a new frame is being digitized. This double buffering capability allows video display at 30 frames per second.

The AG-5 has four basic operations that can be performed within one frame period. These operations are

- 1) Capture a frame to one of the frame buffers and the accumulation buffer
- 2) Add a frame to the contents of the accumulation buffer
- 3) Divide the accumulation buffer by a constant in the range 1 - 127
- 4) Scale the contents of the accumulation buffer to the range 0 - 255.

The last two operations return their result to one of the 8 bit frame buffers and leave the contents of the accumulation buffer unchanged.

The following sections will describe in detail the various components of the AG-5. The Programming Information section of this manual will present specific information for controlling the AG-5 and taking advantage of all the AG-5's features.

Video and Sync Multiplexors

The AG-5 accepts up to four video sources via its 9 pin D shell connector. The individual sources are terminated with 75 ohm resistors upon entering the board. After termination the video signals are routed to two separate four to one multiplexors. The first multiplexor determines which of the video signals will be digitized, while the second multiplexor determines from which of the video signals the necessary video sync information will be obtained. The source selections for digitization and sync are determined by bits in Control Register 3.

Allowing the sync information to be selected from any source provides for capturing flexibility using a simple standard cable assembly. Grayscale video can be captured from any source by selecting the same source for both digitizing and sync information. Color cameras can be connected to the AG-5 using either a separate sync or a sync on green format with the same cabling. Additionally, the AG-5 can be easily integrated into systems that are driven by one or more external sync signals.

Analog to Digital Converter

The selected video signal is next amplified by a factor of three and DC restored by clamping the video sync tips to 0 volts. This amplification improves both the AG-5's signal to noise ratio and the linearity of the analog to digital converter. The video signal is then fed into the analog to digital flash converter. The flash converter converts the incoming video signal into an 8 bit digital value. The analog to digital converter has two analog inputs – top of range and bottom of range – that specify the limits of digitization. If the incoming signal is greater than or equal to the top of range voltage, it will receive a digital value of 255; conversely, an input less than or equal to the bottom of range voltage will receive a digital value of 0.

The top of range and bottom of range voltages are set by two digital to analog converters. These converters have a resolution of 8 bits and are specified by Control Register 4 and Control Register 5, respectively. Each range voltage can be set from 0 volts to 4 volts. The variability of the range of digitization of the analog to digital converter allows the AG-5 to be adjusted to differing input signals by changing the range voltages. For example, if the input signal is low, the range voltages can be lowered to brighten up the captured image. Similarly, if the video signal has poor contrast, the range voltages can be squeezed closer together to increase the contrast in the captured image. Thus control of the range of digitization provides an analog offset and gain capability.

Input Look-up Table

Once the video signal is digitized, the digital data is immediately passed through an input look-up table. The look-up table affords an opportunity to perform some processing on the digitized image such as image inversion and histogram equalization. The look-up table consists of a memory array which maps each of the 256 possible pixel values to a new value (also one of 256).

The primary purpose of the look-up table is to invert the pixel values so as to make the incoming image compatible with the Macintosh. The video is digitized by the analog to digital converter with white receiving a digital value of 255 and black receiving a value of 0. The Macintosh, however, interprets grayscale values in the opposite manner with black as 255 and white as 0. Hence the look-up table inverts each pixel (subtracts it from 255) to convert it to the Macintosh representation.

Arithmetic/Logical Operation Look-up Table

After the digitized data is processed by the input look-up table, it proceeds through the arithmetic/logical operation look-up table. This is a RAM look-up table with an organization of 64 K x 8 bits. Hence there are 65536 entries in this table, each 8 bits wide. The 16 bit address for this look-up table is formed from the 8 bits of digitized data and the eight bits of the corresponding pixel from one of the 8 bit frame buffers. This look-up table thus allows the AG-5 to perform operations between an incoming video frame and a frame stored in one of the frame buffers.

Note that this look-up table can be used to perform any binary (two operand) operation between incoming video and a stored reference frame depending on how the look-up table is loaded. It can be configured to perform, for example, subtraction of a stored frame from incoming video, blank field shading correction, or multiplication (with scaling) of incoming video by a stored frame. The Programming Information section of this manual will provide details for loading this look-up table.

The arithmetic/logical operation look-up table may be bypassed for applications that do not require it. Thus if it is not employed, it does not need to be loaded. Control Register 1 determines if this look-up table is to be inserted in the data path.

Accumulation, Division, and Scaling Unit

The digitized data next proceeds to the Accumulation, Division and Scaling Unit. This component of the AG-5 performs the four basic operations of the AG-5 discussed above. It either passes the digitized data unaltered to one of the frame buffers and the accumulation buffer, adds the incoming frame to the accumulation buffer, divides the contents of the accumulation buffer by a constant, or scales the accumulation buffer to the range 0 - 255. The operation to be performed is specified by Control Register 1.

The Accumulation, Division, and Scaling Unit performs division according to the formula

$$\text{Result Pixel} = \text{Accumulated Pixel} / \text{Constant}$$

where Constant is determined by Control Register 2. The formula for scaling the accumulation buffer is

$$\text{Result Pixel} = (\text{Accumulated Pixel} - \text{Min Pixel}) * 253 / (\text{Max Pixel} - \text{Min Pixel}) + 1.$$

Min Pixel and Max Pixel are determined by the Accumulation Minimum and the Accumulation Maximum Registers respectively. Note that this formula will actually scale the accumulation buffer to the range 1 - 254. All pixels in the accumulation buffer with values below Min Pixel will be set to 0 and all pixels with values above Max Pixel will be set to 255.

The Accumulation Maximum Register and the Accumulation Minimum Register are automatically loaded with the maximum and minimum 15 bit pixel values after either a frame capture operation or a frame accumulation operation. These registers may also be set by software. Hence the scaling process may be flexibly controlled by setting these two registers.

Buffers

The processed image data from the Accumulation, Division and Scaling Unit, either 8 or 15 bits depending on the operation performed, next is stored in one of the buffers. There are four 8 bit frame buffers and one 15 bit accumulation buffer. In a frame capture operation the data is stored in one of the frame buffers, and in the accumulation buffer. In an accumulation operation, the accumulated pixel data is stored in the accumulation buffer. The lower 8 bits of each accumulated pixel is stored in one of the frame buffers. In a division operation or a scaling operation the resultant data is stored in one of the frame buffers and the accumulation buffer is unaltered.

The 8 bit frame buffers are configured as an array of 512 rows of 1024 bytes. As each line of video contains only 640 (768 for CCIR) pixels, each one byte, each row of the frame buffer will contain video data padded at the end with 384 (256) bytes of unused data. Similarly, the last 32 (0) rows of each frame buffer will be unused.

The 15 bit accumulation buffer is configured as an array of 512 rows of 2048 bytes. As each line of accumulated data contains only 640 (768 for CCIR) 15 bit pixel values, each two bytes, each row of the frame buffer will contain accumulation data padded at the end

with 768 (512) bytes of unused data. Similarly, the last 32 (0) rows of the accumulation buffer will be unused.

The frame buffers can be addressed through one of two PCI addresses, corresponding to two separate base address registers in PCI configuration space. Address Space 0 contains a single logical frame buffer into which any of the physical frame buffers may be mapped. Control Register 6 determines which physical frame buffer will be accessed in Address Space 0. The same register also determines which buffer will be used to store a captured frame. Address Space 1 contains all of the available frame buffers. It is recommended that all frame buffer operations take place through Address Space 1, as memory caching can be enabled for this space. Enabling caching to a PCI address space in a Power Macintosh will enable PCI burst transactions to that address space, speeding up all frame buffer operations.

Control and Status Registers

The AG-5 has 6 control registers and one status register. As the names imply, the control registers set the parameters for frame capture while the status register reports the results of capture and also properties of the video signal. Each of the registers is eight bits wide. The control registers are write only; the status register is read only.

Control Register 1 controls the capture process. It contains bits for enabling an operation, for setting which field is to be operated on first, for switching between field mode and frame mode, for enabling the external trigger feature, and for specifying the operation to be performed by the AG-5. Control Register 2 determines the constant to be used by the division operation. Control Register 3 specifies which of the video sources is to be digitized and which of the sources is to be used for sync information.

Control Registers 4 and 5 set the two digital to analog converters on the AG-5. The DAC which determines the top of range voltage for digitization is set by Control Register 4. The DAC which determines the bottom of range voltage for digitization is set by Control Register 5.

Control Register 6 determines which of the frame buffers will be used for capture, which will be mapped into Address Space 0, and which will be input to the arithmetical/logical look-up table.

The AG-5's Status Register contains a bit which reports when an operation has been completed. It also contains two bits which represent timing characteristics of the video sync signal. One bit tells when the video signal is in a vertical sync period. The other bit reports whether the video signal is currently transmitting the even or odd video field.

Programming Information

Introduction

The AG-5 is designed to be easy to program. This section sets forth the details of the AG-5's programming interface and hardware interfacing— its name registry classification, address spaces, register descriptions, and I/O connections. The material presented here should be sufficient to enable an experienced Macintosh programmer to utilize the AG-5 in a custom application.

Programming the AG-5 to capture a video frame is essentially a 7 step process:

- 1) Find the AG-5 using the supplied library routine
- 2) Load the input look-up table
- 3) Set the top and bottom voltages for the digitization range
- 4) Set the Operation Enable bit in Control Register 1
- 5) Wait for the Operation Done bit in the Status Register to come on
- 6) Clear the Operation Enable bit
- 7) Read out the video data from the frame buffer.

Note that for simple applications, it is not necessary to set all parameters, such as selecting the video and sync channels and the frame buffer to be used for capture, as the Control Registers all default to zero on power-up.

For those who need additional guidance in programming with the AG-5, the supplied source code for the Scion Image application software provides a wealth of example code for controlling the AG-5. The source code is written in Pascal using the Metrowerks CodeWarrior development environment. Below is a short list of instructive functions and the files they reside in:

LookForFrameGrabbers:	Init.p
SetupFGPort:	Init.p
ResetScionAG5:	Utilities.p
GetFrame:	Camera.p
CaptureAndDisplayFrame:	Camera.p
Average Frames	Camera.p

There are other routines in these files that perform more specialized functions with the AG-5; a few hours examining the code should prove helpful in learning how to program the AG-5.

On the AG-5 diskette is a C library, ScionLib, which contains a routine that will find the AG-5 in a PCI Macintosh, and return the base addresses for the two address spaces, as well as the number of frame buffers installed on the AG-5. The routine has the form

```
LookForPCIFrameGrabbers(short model, long* base0, long* base1, long* buffers  
                        long* revision).
```

The routine should be passed 3 as the model parameter (this specifies searching for an AG-5), and will pass the base addresses for the two address spaces and the number of buffers and the board revision level in the other parameters. The routine will return true if a

board is found, false otherwise. The routine also enables memory space accesses to the AG-5 and enables memory caching to Address Space 1.

Name Registry Classification

Upon startup a PCI Power Macintosh will create a Name Registry entry for the AG-5. This entry will have a name property value of 'pci11ff,3'. The AG-5 can be located in the Macintosh by searching for a registry entry with this name property. However, this information is not necessary to work with the AG-5 as the library routine discussed above will take care of locating the board.

Address Space

Let us denote the base addresses for the address spaces base0 and base1. Address Space 1 of the AG-5 contains the frame buffers and the accumulation buffer, while Address Space0 contains an alias of one of the buffers, the input look-up table, the arithmetic/logical operation look-up table, the Accumulation Minimum and Maximum registers, the Control Registers, and the Status Register.

The four frame buffers and the accumulation buffer are located in Address Space 1 at

base1	Frame Buffer 0
base1 + \$80000	Frame Buffer 1
base1 + \$100000	Accumulation Buffer
base1 + \$200000	Frame Buffer 2
base1 + \$280000	Frame Buffer 3

When a frame is captured into one of these frame buffers it is stored as a pixel map with a row length of 1024 bytes. The accumulation buffer is represented as a pixel map with a row length of 2048 bytes. The frame buffers and the accumulation buffer may also be accessed in Address Space 0 at address base0 as specified by Control Register 6. The accumulation buffer is accessed at this address as two sections, with the first section corresponding to addresses base1 + \$100000 through base1 + \$17ffff and the second section corresponding to addresses base1 + \$180000 through base1 + \$1ffff.

The input look-up table appears at address base0 + \$e0000. The input look-up table uses only byte lane 0, hence the 256 bytes of the look-up table are addressed at

base0 + \$e0000
base0 + \$e0004
base0 + \$e0008
.
.
.
base0 + \$e03fc.

The lowest address corresponds to the lowest digitization value; i. e. address base0 + \$e0000 maps \$00 (black) pixels, while base0 + \$e03fc maps \$ff (white) pixels.

The arithmetic/logical operation look-up table appears at address base0 + \$80000. This look-up table uses only byte lane 0, hence the 65536 bytes are addressed at

base0 + \$80000

base0 + \$80004
base0 + \$80008
.
.
.
base0 + \$bffc.

Each entry in this table is specified by a 16 bit value of which the upper 8 bits is a pixel in one of the frame buffers and the lower 8 bits is an incoming video pixel. The formula which will determine the proper address in the table for a certain combination of stored pixel and incoming pixel is

$$\text{Address} = \text{base0} + \$80000 + \text{Stored Pixel} \ll 10 + \text{Incoming Pixel} \ll 2$$

where "<<" represents a left bit shift.

The Accumulation Maximum and the Accumulation Minimum Registers are 15 bit read/write registers located at base0 + \$d0000 and base0 + \$d0004, respectively. After the AG-5 performs either a frame capture operation or an accumulation operation, these registers will contain the maximum and minimum accumulated pixel values. The values in these registers control the scaling of the accumulation buffer. When the AG-5 performs a scaling operation, all 15 bit pixel values in the accumulation buffer that fall between (inclusively) the minimum and maximum values represented by these registers will be linearly scaled to the range 1 - 254. All accumulation buffer pixel values which are less than the Accumulation Minimum Register will be given a pixel value of 0; all accumulation buffer pixel values which are greater than the Accumulation Maximum Register will be given a value of 255. These registers may be updated by software at any time. They will only be overwritten by the AG-5 on a frame capture operation or an accumulation operation.

The Control Registers are eight bit wide write-only registers at the following addresses:

CR1: base0 + \$c0000
CR2: base0 + \$c0004
CR3: base0 + \$c0008
CR4: base0 + \$c000c
CR5: base0 + \$c0010
CR6: base0 + \$c0010

The Status Register is an eight bit wide read-only register located at address base0 + \$c0000.

Control and Status Registers

The format of Control Register 1, from most significant bit to least significant bit, is as follows:

CR1_7: Operation Enable
CR1_6: Single Field Select
CR1_5: Starting Field Select
CR1_4: Trigger Enable
CR1_3: Open Drain Output
CR1_2: Arithmetic/Logical Enable

CR1_1: Operation Select MSB
CR1_0: Operation Select LSB.

When Operation Enable is set, the AG-5 will perform one of its four operations during the next incoming video frame. Note that this bit must be reset by software before any additional operations can be performed. It acts as a trigger for a single operation. Operations begin at the trailing edge of vertical sync. When Starting Field Select is set, the specified operation will begin with the odd field; when it is clear, it will begin with the even field. When Single Field Select is set, the specified operation will be performed on only one field — that specified by the Starting Field Select bit. Single fields are captured into the frame buffers as if they were a component of an entire frame; that is, they will load into every other line of the buffer leaving the remaining lines unaltered. When Trigger Enable is set, the AG-5 will wait for a trigger event on the external trigger pin of the video connector before performing an operation. A trigger event is defined as a falling TTL edge. The Open Drain output is available for custom use. The Arithmetic/Logical Enable bit determines if the arithmetic/logical operation look-up table will be used. If this bit is high, the look-up table will be inserted in the data path. The Operation Select bits specify which of the four basic operations the AG-5 will perform as follows:

00: Frame Capture
01: Frame Accumulation
10: Accumulation Buffer Division
11: Accumulation Buffer Scaling

The format of Control Register 2, from most significant bit to least significant bit, is as follows:

CR2_7:
CR2_6: Division Constant MSB
CR2_5: Division Constant
CR2_4: Division Constant
CR2_3: Division Constant
CR2_2: Division Constant
CR2_1: Division Constant
CR2_0: Division Constant LSB.

This register contains the constant to be used in a accumulation buffer division operation. Valid values are in the range 1 - 127. The constant used for division should be the number of frames accumulated by the AG-5 in accumulation operations. Division of the accumulation buffer by values other than the actual number of frames accumulated may give incorrect results.

The format of Control Register 3, from most significant bit to least significant bit, is as follows:

CR3_7: Sync Select MSB
CR3_6: Sync Select LSB
CR3_5: Source Select MSB
CR3_4: Source Select LSB
CR3_3: Frame Buffer Store Select (NuBus Compatibility)
CR3_2: Frame Buffer Feedback Select (NuBus Compatibility)
CR3_1: Frame Buffer Access Select MSB (NuBus Compatibility)
CR3_0: Frame Buffer Access Select LSB. (NuBus Compatibility)

The Source Select bits determine which of the four video sources will be selected for capturing, while the Sync Select bits determine which of the four video sources will be used for sync information. In most cases the same source will be selected for both fields. The lower four bits in this register are provided for software compatibility of programs written for the NuBus version of the AG-5. These buffer control bits may be used instead of those in Control Register 6. Note, however, that if these bits are used, then only two of the frame buffers will be available. The Frame Buffer Store Select bit determines in which 8 bit frame buffer the results of an operation will be stored. If this bit is low, the frame will be stored in Frame Buffer 0, else it will be stored in Frame Buffer 1. The Frame Buffer Feedback Select bit determines which 8 bit frame buffer will be used as an input to the arithmetic/logical operation look-up table. Once again, a low state indicates Frame Buffer 0 and a high state Frame Buffer 1. The Frame Buffer Access bits determine which of the buffers appears in Address Space 0. The bits are interpreted as follows:

00:	Frame Buffer 0
01:	Frame Buffer 1
10:	Accumulation Buffer (base1 + \$100000 to base1 + \$017ffff)
11:	Accumulation Buffer (base1 + \$180000 to base1 + \$1ffff)

Control Registers 4 and 5 control the two digital to analog converters on the board. They accept an integer in the range 0 to 255. The functions of each converter and its voltage range are as follows:

CR4:	Top of Digitization:	0 to 4 volts
CR5:	Bottom of Digitization:	0 to 4 volts

In each case the lower voltage corresponds to register value \$00, while the higher voltage corresponds to register value \$ff. When setting the digitization range, note that the sync tips of the incoming video are clamped to 0 volts and that the video is amplified by a factor of three. Also, for proper operation, the top of digitization voltage must be higher than the bottom of digitization voltage.

The format of Control Register 6, from most significant bit to least significant bit, is as follows:

CR6_7:	Buffer Register Enable
CR6_6:	Frame Buffer Access Select MSB
CR6_5:	Frame Buffer Access Select
CR6_4:	Frame Buffer Access Select LSB
CR6_3:	Frame Buffer Store Select MSB
CR6_2:	Frame Buffer Store Select LSB
CR6_1:	Frame Buffer Feedback Select MSB
CR6_0:	Frame Buffer Feedback Select MSB

This register is new to the PCI version of the AG-5. When the board is reset at power on, this register is not enabled, and the buffer select bits in Control Register 3 are active. Note that Control Register 3 only allows access to the first two frame buffers. Control Register 6 allows the use of all four frame buffers. To enable this register, set the Buffer Register Enable bit high. Then the buffer configuration of the AG-5 may be specified by this register. The Frame Buffer Access bits determine which of the buffers appears in Address Space 0. The bits are interpreted as follows:

000:	Frame Buffer 0
001:	Frame Buffer 1

010:	Accumulation Buffer (base1 + \$100000 to base1 + \$017ffff)
011:	Accumulation Buffer (base1 + \$180000 to base1 + \$1ffff)
100:	Frame Buffer 2
101:	Frame Buffer 3

The Frame Buffer Store Select bits determine in which 8 bit frame buffer the results of an operation will be stored, Frame Buffer 0 through Frame Buffer 3. Similarly, the Frame Buffer Feedback Select bits determine which 8 bit frame buffer will be used as an input to the arithmetic/logical operation look-up table.

The format of the Status Register, from most significant bit to least significant bit, is as follows:

SR_7:	Operation Done
SR_6:	50 Hz
SR_5:	Vertical Sync
SR_4:	Field Status
SR_3:	
SR_2:	
SR_1:	
SR_0:	

The Operation Done bit indicates that an operation has been completed. This bit will be cleared when the Operation Enable bit in Control Register 1 is reset. The 50 Hz bit indicates that the AG-5 is a 50 Hz board, compatible with CCIR video. The Vertical Sync bit will be clear during the vertical sync period of the selected video sync source and set otherwise. The Field Status bit will be set during the odd field of the selected video sync source and clear during the even field. This bit will change at the beginning of the vertical sync period.

Connector Pin Assignments

There is one external connector on the AG-5. This connector is a standard female DB-9 connector. It contains signal lines for the four video sources as well as the external trigger. The pin-out is

Pin 1:	Video Source 3
Pin 2:	Open Drain Output
Pin 3:	Video Source 2
Pin 4:	
Pin 5:	Video Source 1
Pin 6:	
Pin 7:	Video Source 0
Pin 8:	Ground
Pin 9:	External Trigger.

Questions and Answers

Q: Why do I see a cross-hatched interference pattern in the captured image?

A: You are probably trying to capture images from a color (NTSC or PAL) camera. The AG-5 is designed to capture images from an RS-170 (or CCIR) video source. RS-170 (CCIR) is grayscale video. Color video has color information modulated on the grayscale portion of the video signal. This color information causes the distortion pattern in the captured image.

Q: I am trying to do a color capture in Image. I have an RGB camera connected to the AG-5 with the four source cable, but I seem to be having difficulty getting the AG-5 to sync to the camera. What could be causing this?

A: You need to have the 'Separate Sync' box selected in the 'Video Control' dialog box. This dialog box is found under the 'Special' menu. Separate sync tells the AG-5 to look for sync information on the sync signal of the four source cable.

Q: When I try to average a sequence of frames at video rate with Scion's modified version of Image, the software tells me that the sequence is actually averaged at a slower rate. Why can't I average in real-time?

A: If your Macintosh is busy with some background task when you try to average, the AG-5 may not be able to average in real-time. Situations that may slow real-time averaging include network activity such as AppleShare. Try turning off such background tasks while averaging.

Q: How can I capture grayscale images from an RGB camera?

A: There are two methods for capturing grayscale images from an RGB camera. The first is to simply capture from the green signal (source 2 in the 'Video Control' dialog box). The green signal contains the majority of the grayscale information of a color image. The second method is use Image's 'Capture Color' command. After the three color slices are captured, choose the 'RGB to 8 bit Color' command with the existing palette option selected. If you were currently working with a grayscale look-up table, then the resulting image will be the correct grayscale image.

Optional Cables

The AG-5 comes with a Cab-SS-AG5 single source cable suitable for connecting to a grayscale video camera. A number of additional cables are available for connecting to other sorts of cameras and devices:

Cab-RGB-AG5 – This cable, terminated in four BNC connectors, can be used to connect the AG-5 to four separate grayscale video sources. It may also be used to connect to RGB video sources with separate connections for red, green, blue, and sync.

Cab-SVHS-Adp – This adapts any BNC terminated cable to an SVHS connector.

Cab-SST-AG5 – This cable is similar to the supplied single source cable but, in addition, has a BNC connector for the AG-5's external trigger input.

Cab-Int-AG5 – This cable connects the AG-5 to the integration input of the Dage CCD-72 camera.

Cab-Cohu-Adp – This adapts the Dage integration cable for Cohu 491X cameras.

Optional cables are available direct from Scion. We can also manufacture custom cables for use with video sources with non-standard connectors.

Software Support

AxoVideo

AxoVideo is a program for video microscopy that automates both the acquisition and processing of time-lapse images. Acquisition methods include averaging, specifying regions-of-interest (ROI), "zones" that quantify average intensities of ROI's, and a line scan "composite-time image" for fast changing intensities. Dual-image acquisition operations are available with foreground/background control for subtraction, merging and ratioing of images. There are many filtering convolutions, as well as pseudo-coloring, directional measurements and annotations. Macro recording is built-in. AxoVideo includes hardware device support for frame grabbers, such as the Scion AG-5, stage controllers, shutter controllers and a filter wheel. AxoVideo runs on the Apple Macintosh II and Quadra computers.

Axon Instruments, Inc.
1101 Chess Dr.
Foster City, CA 94404
(415) 571-9400.

IPLab Spectrum-AG5

IPLab Spectrum-AG5 software provides scientific imaging, visualization, analysis, image acquisition and laboratory automation in a single package. This version of IPLab controls all features of Scion's AG-5 frame grabber. Applications include microscopy, low-light imaging, bio-medicine, and others. Signal Analytics provides specific solutions based on this board for low-cost fluorescence imaging applications, including ion ratio imaging and fluorescence in situ hybridization. With IPLab you can: automatically analyze particles; perform FFTs, image enhancement, densitometry and morphometry; acquire, deconvolve, and display 3-D serial sections; control lab equipment such as motorized stages and filter wheels. You can also use IPLab as a development environment for new algorithms by adding your own code written in C or Pascal. Custom software development is also available from Signal Analytics.

Signal Analytics Corporation
440 Maple Ave. East
Suite 201
Vienna, VA 22180
(703) 281-3277

NIH Image

NIH Image is a public domain image processing and analysis program for the Macintosh. It can acquire, display, edit, enhance, analyze, print, and animate images. It reads and writes TIFF, PICT, PICS, and MacPaint files, providing compatibility with many other applications, including programs for scanning, processing, editing, publishing, and analyzing images. It supports many standard image processing functions, including contrast enhancement, density profiling, smoothing, sharpening, edge detection, median filtering, and spatial convolution with user defined kernels up to 63x63. NIH Image also incorporates a Pascal-like macro programming language, providing the ability to automate complex, and frequently repetitive, processing tasks.

National Technical Information Service
5382 Port Royal Rd.
Springfield, VA 22161
(703) 487-4650

Ultimage

Ultimage is a powerful image processing and analysis tool that takes full advantage of the graphic capabilities and user interface of the Macintosh II. It offers a complete library of image processing functions that can be used for a large variety of applications. The program can process images acquired from scanners, cameras, microscopes, and other acquisition systems. Several images of different formats can be displayed and manipulated simultaneously, using either the 256 gray levels or the color capabilities of the Macintosh. The main features of Ultimage include image enhancement, thresholding, zooming, contour detection, histogram manipulation, palette modification, 3D display, and arithmetic and logic operations. A set of advanced functions is also available for scientific and professional image processing such as morphology analysis, pattern recognition and classification, frequency domain analysis, and linear and non-linear filtering.

GTFS, Inc. (West Coast)
2455 Bennet Valley Rd. #100C
Santa Rosa, CA 95404
(707) 579-1733

Engineering Technology Center (East Coast)
240 Oral School Rd. Suite 105
Mystic, CT 06355
(800) 959-3011

Concept VI

Concept VI is a package of libraries compatible with the LabVIEW graphical programming and instrumentation software from National Instruments. Each library includes various groups of functions ranging from image display utilities and fundamental image processing to advanced quantitative analysis. These libraries include time-lapsed and triggered image acquisition, automatic image indexation, filing and archiving, basic densitometry analysis, automated image processing, object identification and measurement, feature-based labeling, data collection, and statistical and frequency domain analysis.

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Video VI

The Video VI package supports video data acquisition and image manipulation in the LabVIEW environment for the Macintosh. LabVIEW is the graphic and object oriented

instrumentation software from National Instruments. The Video VI package is a cost effective alternative for building systems that require image acquisition, analysis, and documentation in process control environments. There are currently over 20 VI's (Virtual Instruments) in the Video VI package. These include VI's for capturing images with the Scion AG-5, reading and writing TIFF files, displaying images, moving and scaling images, and thresholding.

GTFS, Inc.
2455 Bennet Valley Rd. #100C
Santa Rosa, CA 95404
(707) 579-1733

Specifications

Imaging

Pixel Depth: 8 bits
Image Resolution: 640 x 480 (768 x 512) pixels
Pixel Aspect Ratio: 1 to 1

Capturing

Functions: capture, sum, divide, scale
Function Speed: 1/30 (1/25) second
Function Mode: field or frame
Initial Field: even or odd

Memory

Frame Buffers: 4, 8 bit
Accumulation Buffers: 1, 15 bit

Look-up Tables

Input Look-up Tables: 1, 256 x 8
Arithmetic Look-up Tables: 1, 64K x 8

Video Interface

Input Sources: 4, AC coupled
Video Input Level: 1 volt peak to peak
Video Signal Type: RS-170 (CCIR)
Video Gain Factor: 3
Digitizing Range, Bottom: 0 to 4 volts
Digitizing Range, Top: 0 to 4 volts
External Trigger: TTL falling edge

Connectors

Video Connector: 9 pin D shell

General

Installation: 1 PCI slot (full size)
Operating Conditions : 0 to 70° C
Power: 15 watts typical

Warranty and Support

Limited Warranty

Scion Corporation ("Scion") warrants this AG-5 against defects in materials and workmanship for a period of one (1) year from the date of original purchase. If you discover a defect, Scion will, at its option, repair, replace, or refund the purchase price of this AG-5 to you, provided you return it during the warranty period, with transportation charges prepaid, to Scion. Each AG-5 returned for warranty service must bear a Return Materials Authorization number, which may be obtained from Scion, on the outside of the shipping box.

This warranty does not apply if the product has been damaged by accident, misuse, or misapplication; if the product has been modified without the written permission of Scion; or if the AG-5 serial number has been removed or defaced.

THE WARRANTY AND REMEDIES SET FORTH ABOVE ARE EXCLUSIVE AND IN LIEU OF ALL OTHERS, WHETHER ORAL OR WRITTEN, EXPRESS OR IMPLIED. SCION SPECIFICALLY DISCLAIMS ANY AND ALL IMPLIED WARRANTIES, INCLUDING, WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. NO SCION DEALER, AGENT, OR EMPLOYEE IS AUTHORIZED TO MAKE ANY MODIFICATION, EXTENSION, OR ADDITION TO THIS WARRANTY.

Scion is not responsible for special, incidental, or consequential damages resulting from any breach of warranty, or under any other legal theory, including but not limited to lost profits, downtime, goodwill, and damage to or replacement of equipment and property.

Some states do not allow the exclusion or limitation of incidental or consequential damages or exclusions of implied warranties, so the above limitations or exclusions may not apply to you. This warranty gives you specific legal rights, and you may also have other rights that vary from state to state.

Money-Back Guarantee

You may return your AG-5 to Scion Corporation, within 30 days of the date of invoice, for a full refund of the purchase price. All returns must be in as new condition and be returned with all supplied accessories in the original shipping box. All returns must bear a Return Materials Authorization number, which may be obtained from Scion, on the outside of the shipping box.

If payment has already been made at the time you return your AG-5, a cash refund will be made within 30 days of Scion's receipt of the AG-5. If payment has not been made at the time Scion receives your AG-5, a credit memo will be issued against the outstanding invoice within 15 days of Scion's receipt of the AG-5.

Service Information

Should you determine that your AG-5 requires service, it should be returned directly to Scion Corporation for repair. Before returning your AG-5, call Scion for a Return Materials Authorization number. This number should be printed on the outside of the

shipping carton. Carefully pack the AG-5 in its original shipping materials and include a short note describing the problem. You are responsible for all shipping costs to Scion and for insuring the returned unit. Scion will commit its best efforts to repairing your unit within 5 days of receipt of the unit at our factory.

If your AG-5 is under warranty, it will be repaired or replaced at no charge. Scion will pay for shipping your AG-5 back to you by ground transportation. You may, at your cost, request faster transportation. If your AG-5 is not under warranty, there will be a minimum repair charge of \$150. If the repair cost is greater than \$150, you will be called to approve the necessary work. You must provide, in advance, appropriate payment information (e.g., approved purchase order, credit card number) for non-warranty repair work.